Fabrication of recessed-gate AlGaN/GaN MOSFETs using TMAH wet etching with Cu ion implantation

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Abstract

In this study, recessed-gate AlGaN/GaN MOSFETs were fabricated using a novel recess etching method—TMAH wet etching with Cu ion implantation. This innovative approach injects Cu ions selectively into the target AlGaN layer, creating defects that are then etched with a TMAH solution, dissolving Ga along with the defect. Compared to the conventional GaN recess etching method of ICP-RIE dry etching, TMAH wet etching offers more precise etching without causing plasma damage on the etched surface. To demonstrate the superiority of TMAH wet etching, devices fabricated with this method were analyzed and compared with devices fabricated using ICP-RIE dry etching. The AFM images of the etched surface demonstrated the superior stability of TMAH wet etching. In addition, electrical characteristics measurements revealed that the devices using TMAH wet etching exhibited a higher on-current (295.05 mA/mm), lower gate lag rate (15.98%), and a higher breakdown voltage (733 V) than ICP-RIE etched devices.

Keywords: AlGaN/GaN heterojunction; Ion implantation; Enhancement mode high electron mobility transistor (E-mode HEMT); GaN power device

1. Introduction

The significance of energy as a social infrastructure is crucial for humanity. Advancements in harnessing renewable resources such as wind, solar, geothermal, and bioenergy necessitate various power conversion systems. Addressing voltage blocking and conversion efficiency challenges is pivotal, with wide bandgap semiconductors playing a key role. Consequently, developing power systems around these semiconductors has emerged as a challenging yet essential pursuit. Gallium nitride (GaN) based power transistors are attracting attention because they meet the conditions for innovation.

AlGaN/GaN high-electron-mobility transistors (HEMT) offer low on-resistance ($R_{on}$) attributed to two-dimensional electron gas (2-DEG), providing advantages in high-power and high-frequency applications [1-10]. Noteworthy strengths of these devices include a high critical electric field, high electron mobility, and resilience to high temperatures [11-14]. Despite these merits, AlGaN/GaN HEMTs have limitations. First, the absence of an insulating oxide layer between the semiconductor and the gate metal leads to a gate leakage current. Second, their normally-on characteristics allows current flow without a gate voltage, resulting in poor stability due to complicated circuits.

To solve these problems, extensive research has been conducted. The development of a metal-insulator-semiconductor (MIS) structure has been instrumental in mitigating gate leakage current [15-22]. Various techniques have emerged to achieve normally-off operation, including the use of a p-type doped GaN gate or regrowth of p-GaN [23], fluorine treatment [24], and physically etching the AlGaN layer beneath the gate using inductively coupled plasma-reactive ion etching (ICP-RIE) dry etching [25]. However, these methods encounter significant problems. Fluorine treatment causes strong plasma damage on the AlGaN/GaN surface, p-type doping faces challenges in dopant activation, p-GaN regrowth is hindered by cost concerns, and ICP-RIE dry etching suffers from low precision and plasma damage.

This study employs an MIS structure to minimize gate leakage current and uses a recessed gate structure to implement a normally-off operation. A novel etching approach, tetramethylammonium hydroxide (TMAH) wet etching using Cu ion implantation, was introduced. This method leverages the property of TMAH solution to dissolve Ga atoms and defects [26-29]. By creating a defect with a Cu ion beam in the target, only the desired AlGaN layer is etched during TMAH wet etching. This etching method offers high precision and avoids plasma damage. We fabricated recessed-gate AlGaN/GaN MOSFETs using the TMAH wet etching technique. In
addition, the devices were fabricated using ICP-RIE dry etching, a commonly used etching method, and the electrical characteristics of the two types of devices were compared.

2. Device fabrication and experimental methods

Figure 1 illustrates a cross-sectional view of the fabricated recessed-gate AlGaN/GaN MOSFET. The devices were fabricated with AlGaN/GaN layers grown on a sapphire substrate using metal organic chemical vapor deposition (MOCVD). The specific epitaxial (epi) parameters include a 25-nm thick AlGaN layer, 180-nm thick undoped GaN layer, 2.1-μm thick high-resistive GaN layer, and 430-μm thick sapphire substrate. Hall measurements revealed a carrier density of $2.26 \times 10^{13} \text{cm}^{-3}$ and an electron mobility of 1120 cm$^2$/V∙s.

Device fabrication was started with the removal of contaminants on the substrate and native oxides, followed by a 5-minute treatment with a buffered oxide etchant (BOE). Device-to-device isolation was achieved by mesa etching ICP-RIE with Cl$_2$:Ar (100:10 sccm) gas for 150 s, resulting in an etched depth of 400 nm. The mesa region was patterned by GXR 601 positive photoresist, as shown in Figure 2, which illustrates the schematics of the gate recess etching process after the mesa etching process. The process involved the formation of a hard mask to selectively inject Cu ions into the gate region for recess etching. A 100-nm thick Si$_3$N$_4$ layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). The Si$_3$N$_4$ layer at the gate region was removed by BOE, followed by the redeposition of a 40-nm thick Si$_3$N$_4$ layer to passivate the ion beam implantation damage. Subsequently, Cu ion beam implantation was conducted with an energy of 30 keV and a fluence of $10^{15} \text{cm}^{-2}$. After implantation, the Si$_3$N$_4$ layer was removed using BOE. A 15-nm thick HfO$_2$ layer was deposited for passivation from TMAH. The HfO$_2$ passivation layer at the gate foot region was etched away using ICP-RIE with CF$_4$:Ar (100:10) gas. The target AlGaN layer beneath the gate region was recessed using TMAH solution (5% concentration at 80 °C) for 10 min. After AlGaN layer removal, the surface of the high-resistive

![Fig. 1. Cross-sectional view of the fabricated recessed-gate AlGaN/GaN MOSFET.](image)

![Fig. 2. Schematics of the gate recess etching process: (a) Cu ion beam implantation with Si3N4 hard mask, (b) TMAH wet etching with HfO2 hard mask, and (c) after TMAH wet etching.](image)
GaN layer was treated with the same TMAH solution to ensure a smooth surface and removal of gallium oxide [30-32]. Subsequently, the HfO$_2$ mask layer was removed by BOE, and the 30-nm thick Si$_3$N$_4$ layer was deposited to protect the GaN surface during the high-temperature ohmic process. A Si/Ti/Al/Ni/Au (1/15/160/40/100 nm) ohmic metal stack was evaporated using an E-beam evaporator and annealed at 900 °C for 50 s in N$_2$ ambient. A 30-nm thick Al$_2$O$_3$ film was deposited as a gate metal insulator using plasma enhanced atomic layer deposition (PE-ALD). Finally, the Ni/Au (30/300 nm) gate electrode was deposited using an E-beam evaporator. The comparative device featured a recessed-gate structure using ICP-RIE dry etching instead of TMAH wet etching, with both types of devices having an identical structure.

3. Results and discussion

To determine the optimal implantation energy before ion implantation, a stopping and range of ions in matter (SRIM) simulation was employed to calculate the distribution of ions irradiated within the substrate and the corresponding vacancy distribution [33]. SRIM comprises computer simulators designed to calculate interactions between ions and matter. The target material comprised a 40-nm thick Si$_3$N$_4$ layer, a 20-nm thick AlGaN layer, and a 50-nm thick GaN layer for passivating ion beam damage. The densities of Si$_3$N$_4$, AlGaN, and GaN are 3.17 g/cm$^3$, 5.5 g/cm$^3$, and 6.1 g/cm$^3$, respectively. The ion beam energy of Cu was 30 keV. Considering the varying ion depth based on ion beam energy and the thickness of the Si$_3$N$_4$ and AlGaN layers, the ion beam energy was carefully chosen. Adjusting the ion beam energy allows control over the depth to be etched. Figure 3(a) shows the trajectory of Cu ions, and Figure 3(b) shows the distribution of Cu ions. Figure 3(c) and 3(d) show the trajectory of vacancies and their distribution, respectively.

![Fig. 3. SRIM calculation of (a) ion trajectory, (b) ion range, (c) vacancy trajectory, and (d) vacancy range due to 30 keV Cu ion beam implantation in the AlGaN/GaN substrate.](image-url)
show the trajectory and distribution of vacancies in the AlGaN and GaN layers resulting from Cu ion implantation. Simulation results indicate that the tail of the vacancy distribution resides in the AlGaN layer, preserving the integrity of the GaN layer without damage.

After the simulation, Cu ions were implanted into the substrate using the ion implanter at the Korea Multi-Purpose Accelerator Complex, employing a 30 keV accelerating voltage and $10^{15} \text{cm}^2$ ion dose. Subsequently, the depth of the injected Cu ions was indirectly verified by exploiting the notable increase in the etching rate caused by vacancies. The AFM images in Figures 4(a)-(d) depict the substrate surface following treatment with TMAH solution (5%, 80 °C) for varying wet etching durations. Over 10 min, the etch depth reached 18 nm at a rate of approximately 2 nm/min. Beyond 10 min, the rate decreased to 0.2 nm/min, resulting in a final etch depth of 20 nm. Subsequently, only the GaN layer remained and exhibited no further etching after 20 min. Consequently, the vacancies penetrated up to a depth of 18 nm.

This study compared the electrical characteristics of recessed gate AlGaN/GaN MOSFETs fabricated by TMAH wet etching and those fabricated by ICP-RIE dry etching. Figures 5(a) and 5(b) show the depth profile of the recessed-gate AlGaN/GaN structure after TMAH wet etching and ICP-RIE dry etching, respectively. The depth of the device subjected to TMAH wet etching was 18 nm, whereas the depth of the device subjected to ICP-RIE dry etching was 21 nm.

![Fig. 4. Depth profiles of the recessed-gate AlGaN/GaN substrate etched by TMAH for (a) 10 mins, (b) 15 mins, (c) 20 mins, and (d) 60 mins.](image)

![Fig. 5. Depth profiles of the recessed-gate AlGaN/GaN substrate (a) by TMAH wet etching and (b) by ICP RIE dry etching.](image)
Figure 6 shows the $I_D$ and transconductance ($g_{mn}$) characteristics of the recessed-gate AlGaN/GaN MOSFETs. The ICP-RIE device demonstrated a maximum drain current ($I_{DS,max}$) of 10.66 mA/mm at 10 V of $V_{GS}$, whereas the TMAH-etched device achieved 241.57 mA/mm. The $g_{mn}$ of the TMAH-etched device surpassed that of the ICP-RIE-etched device by 27 times, accompanied by a $V_{th}$ that was higher by over 0.6 V. This disparity arises from the inherent difficulty in achieving precise etching with ICP-RIE dry etching. During the ICP-RIE dry etching process, a 1-nm over etching occurred due to precision issues, which resulted in the depletion of the two-dimensional electron gas (2-DEG) layer and a very low on-current.

The impact of over-etching on ICP-RIE devices resulted in a smaller on-current and higher off-current, which represent the reduction rates of $I_{DS}$ for the TMAH-etched device exceeded that of the ICP-RIE-etched device by approximately three orders of magnitude.

Figure 7 shows the log-scale $I_{DS}$-$V_{GS}$ transfer curves and $I_{GS}$-$V_{GS}$ curves of the devices. The $I_{on}$-$I_{off}$ ratio of the TMAH-etched device exceeded that of the ICP-RIE-etched device by approximately three orders of magnitude. The gate and drain lag rates, which represent the reduction rates of $I_{DS}$ due to current collapse, were analyzed for the two types of fabricated devices [37-38]. The gate lag rates of the ICP-RIE-etched and TMAH-etched devices were 21.50% and 16.23%, respectively. The higher gate lag rate of the ICP-RIE-etched device was attributed to trap formation from the inherent difficulty in achieving precise etching with ICP-RIE dry etching. During the ICP-RIE dry etching process, a 1-nm over etching occurred due to precision issues, which resulted in the depletion of the two-dimensional electron gas (2-DEG) layer and a very low on-current.

The discrepancy in $R_{on}$, which was higher by over 0.6 V. This disparity arises from gate and surface leakage currents. These leakage currents originated from the traps caused by plasma damage beneath the gate.

Figure 8 illustrates the DC output characteristics of the devices. The on-resistance ($R_{on}$) of each device was extracted from the DC output curve at $V_{DS} = 0.1$ V. The calculated $R_{on}$ was 571.36 Ω-mm for the ICP-RIE-etched device and 35.29 Ω-mm for the TMAH-etched device. The discrepancy in $R_{on}$ mirrors the same factors influencing the earlier observed on-current difference.

Figures 9(a) and 9(b) show the pulsed $I_{DS}$-$V_{DS}$ curves for each device. A gate stress of -2 V and a drain stress of 10 V were applied, using a pulse width of 2 ms and a pulse period of 5 ms [34-36]. The gate and drain lag rates, which represent the reduction rates of $I_{DS}$ due to current collapse, were analyzed for the two types of fabricated devices [37-38]. The gate lag rates of the ICP-RIE-etched and TMAH-etched devices were 21.50% and 16.23%, respectively. The higher gate lag rate of the ICP-RIE-etched device was attributed to trap formation from the inherent difficulty in achieving precise etching with ICP-RIE dry etching. During the ICP-RIE dry etching process, a 1-nm over etching occurred due to precision issues, which resulted in the depletion of the two-dimensional electron gas (2-DEG) layer and a very low on-current.

![Fig. 6. $I_{DS}$-$V_{GS}$ transfer curve and $g_{mn}$ transconductance curve of (a) the ICP etched device and (b) the TMAH etched device.](image)

![Fig. 7. Log-scale $I_{DS}$-$V_{GS}$ transfer curves and $I_{GS}$-$V_{GS}$ curves of the fabricated devices with $L_{GD} = 10 \mu$m.](image)
at the bottom of the gate caused by plasma damage during ICP-RIE etching. The drain lag rate was higher for the TMAH-etched device than for the ICP-RIE-etched device, which stems from differences in the buffer trap quality of the substrates.

Fig. 10 shows the breakdown voltage (BV) curve of the ICP-RIE etching device and TMAH etching device. The breakdown voltage was determined as $10^{-3}$ A/mm of current limit. To maintain the off state, $V_{GS}$ of 0 V was applied, and BV was measured by conducting a drain voltage sweep from 0 V to 1000 V. The BV of the ICP-RIE etched device was 612 V, and the BV of the TMAH etched device was 733 V. The reason why the BV
of the TMAH etched device is higher is that ICP-RIE dry etching causes plasma damage to the bottom of the gate during gate recess etching.

4. Conclusions

In this paper, we introduce a novel recess etching technique, TMAH wet etching with Cu ion implantation. The method was employed to fabricate recessed gate AlGaN/GaN MOSFETs, with a comparison to devices fabricated using the conventional ICP-RIE dry etching method. Subsequently, the electrical characteristics of the two devices were compared and analyzed. Cross-sectional AFM images highlighted the uniformity achieved by TMAH etching on the AlGaN layer, in contrast to ICP-RIE dry etching. Moreover, the precision challenges of ICP-RIE dry etching led to partial over-etching of the target AlGaN layer by approximately 1 nm. Consequently, the complete depletion of 2-DEG in the GaN channel layer resulted in a notably low on-current. Conversely, TMAH wet etching demonstrated precise etching of the AlGaN layer to the target depth, ensuring both normally-off operation and a high on-current. Notably, TMAH wet etching has the advantage of avoiding plasma damage to the gate, which is a concern in ICP-RIE dry etching. These characteristics resulted in a 19.78% higher BV and a 24.53% lower gate lag rate than those of devices fabricated through ICP-RIE dry etching. These results affirm the feasibility of semiconductor etching by controlling defects and improving the reaction of the solution, thereby establishing TMAH wet etching as a method that surpasses existing ICP-RIE dry etching.

5. Authorship contribution statement

J. H. Heo conducted the fabrication, analyzed the data, and wrote the manuscript. S.H. Lee, J. Park, G.E. Kang. Participated in experiments. I.M. Kang and Y.J. Yoon supervised and revised the manuscript. All the authors read and approved the final manuscript.

6. Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

7. Availability of data and materials

Here All data are fully available without restriction.

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9. References


